Fault Diagnosis in Digital Part of Mixed-Mode Circuit

Miona Andrejević, Vančo Litovski and Mark Zwolinski

Abstract – In this paper artificial neural networks (ANNs) are applied to diagnosis of catastrophic defects in the digital part of a nonlinear mixed-mode circuit. The approach is demonstrated on the example of a relatively complex sigma-delta modulator. A set of faults is selected first. Then, *fault dictionary* is created, by simulation, using the response of the circuit to an input ramp signal. It is represented in a form of a look-up table. Artificial neural network is then trained for modeling (memorizing) the look-up table. The diagnosis is performed so that the ANN is excited by faulty responses in order to present the fault codes at its output. There were no errors in identifying the faults during diagnosis.

I. INTRODUCTION

Every complex system is liable to faults or failures. In most general terms a fault is any change in a system that prevents it from operating in the proper manner. We define diagnosis as the task of identifying the cause of a fault that is manifested by some observed behavior. Then some method of determining what fault has occurred is required. This is most often considered to be a two-stage process: firstly the fact that fault has occurred must be recognized – what is referred to as fault detection. Secondly, the nature should be determined such that appropriate remedial action may be initiated.

The explosion of integrated circuit technology has brought with it some difficult testing problems. The recent growth of mixed analogue and digital circuits complicates the testing problem even further. It becomes more complicated to determine a set of input test signals and output measurements that will provide a high degree of fault coverage. There is also a timing problem of testing the circuits even on the fastest automated equipment.

In this paper we will show that feed-forward ANN may be applied to the diagnosis of non-linear dynamic electronic circuits that are mixed with digital ones. In order to make the explanation easier to understand, only a reduced set of faults will be used i.e. catastrophic defects in the digital part of the converter. Only single faults are considered.

The simulation before test concept was adopted. This means that after choosing the set of faults of interest (say the most probable ones), repetitive simulation is performed in order to create the system response for every fault. Codes are associated to the responses and used as part of the fault dictionary that, in addition, contains the faulty responses themselves. Of cause, the responses are represented in a form that is easy to manipulate.

The ANN is first trained for modeling the look-up table. This means that faulty responses are repeatedly brought to the input, while the ANN is forced to present the fault codes at its output. Then, the ANN running with the given vector of stimuli (measured output signals of a faulty or, possibly, fault free system) may be viewed as search of the look-up table. The ANN response, if the network properly trained, will immediately find the fault and produce the fault code at its output.

The procedure applied is reminiscent to the one implemented to analog circuits in [1]. To our knowledge this is the first application of ANNs to diagnosis of mixed signal circuit.

II. CONCEPTS OF DIAGNOSIS

Besides the human expert that is usually performing the diagnostic project, one needs tools that will help, and what is most desired, will perform diagnosis automatically. Such tools are a great challenge to design engineers that pertains to the fact that generally the diagnostic problem is indeterminate. In addition, it is a deductive process with one set of data creating, in general, unlimited number of hypotheses among which one should try to find the solution. This is why permanent attention of the research community is attracted by this problem [2].

During the life-cycle of a product, testing is implemented in both the production phase and the implementation phase. We claim, however, that the sustainability of a product is strongly influenced by the design phase. So, to make a sustainable product, one should design the test procedure and synthesize test signals early in the design phase.

It is frequently possible to perform functional verification of the system. That, most frequently, happens when a small number of input/output terminals is present. In the majority of cases however, full functional testing becomes time consuming and is not acceptable. So, one applies defect-oriented (structural) testing, as will be discussed in more detail as follows.

We consider testing to be: the selection of a set of defects regarded as the most probable, the description of a set of measurements, the selection of a set testing points (or output signals) and most importantly, the synthesis of optimal testing signals that will be applied at the system inputs allowing for detectability and observability of the listed fault effects. Here, optimality means that one test signal covers as many faults as possible.

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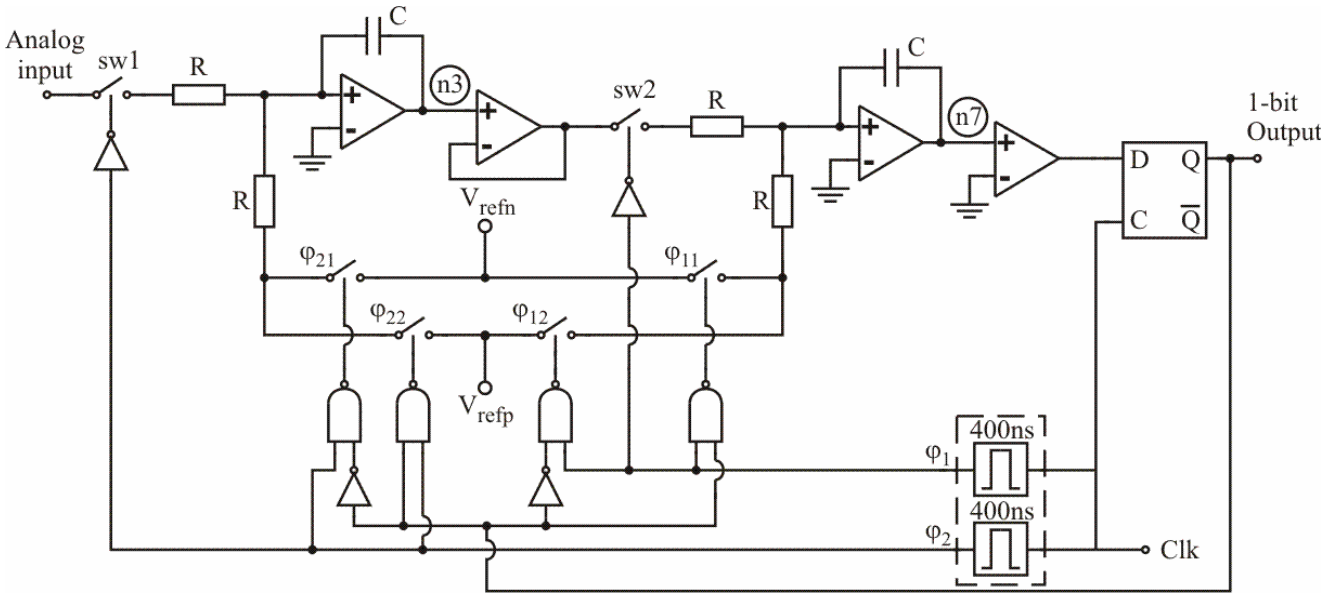

Fig. 1. Sigma-delta modulator architecture.

Selection of the type of measurements and testing points is specific to the circuit. One should stick to those measurements that are prescribed for functional verification. Specific measurements such as supply current monitoring are frequently adopted, too. Separate test points may be added in order to improve detectability or observability. Specific design for testability concepts can be applied.

After selection of test signals, the fault coverage has to be evaluated. To do that, as many replicas of the original circuit as the number of predicted faults have to be created. For large complex systems containing mechanical, analogue and digital parts, the number of replicas becomes huge. Each replica has one fault inserted. The fault coverage is evaluated after simulation of the faulty systems by comparing the results thus obtained with the response of the fault-free system. If these two differ, the fault is covered and the corresponding entry in the fault list can be removed. To reduce the computational effort, algorithms have been proposed to simulate multiple faulty circuits concurrently in both the analogue and the digital domains but not in mixed signal, and mixed description systems.

III. Sigma-delta Modulator Architecture

As an example of a complex non-linear dynamic electronic circuit with mixed signals, the architecture of sigma-delta modulator is chosen.

Sigma-delta modulators are very attractive for design low frequency high-resolution analog-to-digital converters. Sigma-delta modulators trade speed for resolution. They employ coarse quantization in one or more feedback loops. By sampling at a frequency that is much greater than the signal bandwidth, it is possible for the feedback loops to shape the quantization noise so that most of the noise power is shifted out of the signal band. The out of band noise can then be attenuated with a digital filter. The degree to which the quantization noise can be attenuated depends on the order of the noise shaping and the oversampling ratio [3].

In addition to their tolerance for circuit nonidealities, oversampled A/D converters simplify system integration by reducing the burden on the supporting analog circuitry. Because they sample the analog input signal at well above the Nyquist rate, precision sample-and-hold circuitry is unnecessary. Also, the burden of analog antialiasing filter is considerably reduced. Much of its function is transferred to the digital decimation filter, which can be designed and manufactured to precise specifications, including a linear phase characteristic.

IV. Faults in the Specific Modulator Design

As an example of a complex circuit, the sigma-delta modulator in Fig. 1 is chosen [2]. This is a mixed-signal circuit, having both analogue and digital elements. Switches in the circuit are modeled as truly ideal switches, with zero resistance for closed switch and infinite resistance for open switch [4].

The integrator charging time is invariable with respect to clock rate in order to keep the gain constant. This means that the analog switch must be turned on for fixed time duration regardless of clock rate. This is achieved by using monostable multivibrator as a fixed-width pulse generator in the circuit. The monostable multivibrator between the clock input and switch control block functions as a pulse

generator to produce control signals of fixed time duration. Fig. 2 shows reaction of the system when the input is excited by a sinusoidal signal.

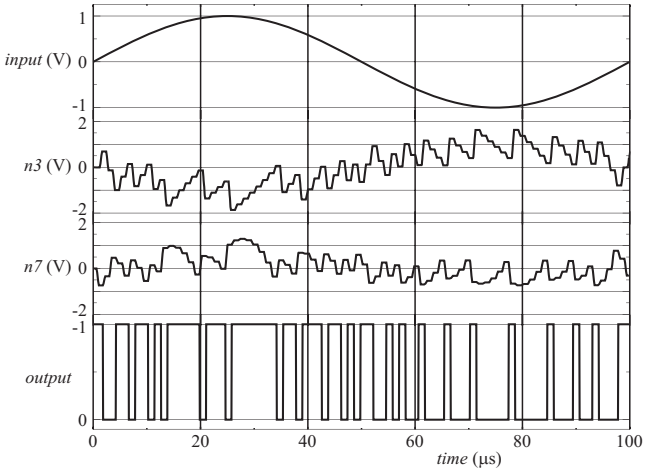

Fig. 2. Simulation results for linear sinusoidal excitation

In this paper only the faults in the digital part of the circuit will be considered. Digital signal can be "stuck-at-1" or "stuck-at-0". In the circuit in Fig. 1, analogue switches are controlled by digital signals, so there are pairs of the same fault effects, such as: the effect is the same when the switch is stuck at ON (OFF) and the logic circuit's output is "stuck-at-1" ("stuck-at-0"). So, we will consider hard faults (which refer to the analogue part of the circuit) as stuck switches.

TABLE I
FAULT DICTIONARY

Type of fault	Signature	Fault code
FF	C9CA9	0
sw_1OFF	99999	1
φ_{12}OFF	38E38	2
φ_{21}OFF	00000	3
φ_{22}OFF	FFFFF	4
sw_1ON	63655	5
φ_{11}OFF	1F07C	6
sw_2ON	E0F83	7
sw_2OFF	AAAAA	8

Fault dictionary is created using the response of the circuit to an input ramp signal. We published one approach to fault dictionary creation, where output signals of the fault-free and of the faulty circuits are transformed using the Fast Fourier Transformation, in [5].

In the alternative approach given here, the circuit output value is registered after every clock period, so these output digital values form the output signature. These are then represented in more compact hexadecimal presentation. Accordingly, fault dictionary is created and shown in Table 1. In the first column of Table 1, eight selected faults are named. FF stands for the fault free circuit. The cases when switches in the feedback loop (φ_{11}, φ_{12}, φ_{21}, φ_{22}) are permanently closed are excluded, because voltage references V_{refp} and V_{refn} would be shorted in such cases. The second column contains the signature seen at the output. The signature is then coded as shown in the third column. In the coding procedure we had in mind that similar responses must not have similar fault codes (for example response 99999 and AAAAA (hexadecimal value *A* is presented to the neural network as decimal value *10,* or F as decimal value *15*)).

TABLE II
ANN WEIGHTS AND THRESHOLDS

weight (1,1)(2,1)	120.812
weight (1,2)(2,1)	-71.5911
weight (1,3)(2,1)	-170.517
weight (1,4)(2,1)	145.099
weight (1,5)(2,1)	10.6883
weight (1,1)(2,2)	104.461
weight (1,2)(2,2)	-85.9051
weight (1,3)(2,2)	-181.814
weight (1,4)(2,2)	142.592
weight (1,5)(2,2)	5.02798
weight (1,1)(2,3)	118.426
weight (1,2)(2,3)	-80.095
weight (1,3)(2,3)	-166.541
weight (1,4)(2,3)	139.481
weight (1,5)(2,3)	-8.45216
weight (2,1)(3,1)	14.4496
weight (2,2)(3,1)	10.0822
weight (2,3)(3,1)	-14.6015
threshold (2,1)	-18.3932
threshold (2,2)	5.31276
threshold (2,3)	0.747092
threshold (3,1)	0.25

Artificial neural network was trained for modeling the look-up table. It is a feed-forward neural network with one hidden layer. The structure of the network is shown in Figure 3. The signatures are inputs to the network, and the fault code is network output to be learned. It means that the neural network has five input (one input per hexadecimal digit) and one output neuron. Hexadecimal values are presented as decimal when they are inputs to the network. After learning was completed, the number of hidden neurons in the resulting ANN was three, what was found by trial and error after several iterations starting with an estimation based on [6] and [7]. Parameters of the obtained network, its weights and thresholds, are presented in Table 2.

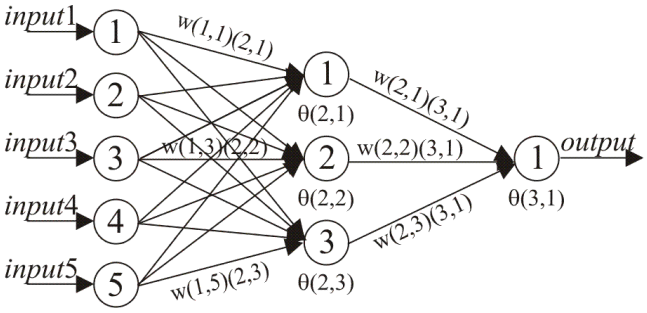

Fig. 3. The structure of the ANN used for diagnosis of digital faults in the circuit in Fig.1.

TABLE III
ANN OUTPUT CODES

Type of fault	Fault code	ANN output
FF	0	0.00754392
sw_1OFF	1	1.00436
φ_{12}OFF	2	2
φ_{21}OFF	3	2.99988
φ_{22}OFF	4	4.00265
sw_1ON	5	5.00078
φ_{11}OFF	6	5.9999
sw_2ON	7	7.0013
sw_2OFF	8	8.00416

The structure and the parameters of the obtained ANN are verified by exciting the ANN with faulty inputs. Responses of the ANN show that there were no errors in identifying the faults what is presented in Table 3. Negligible discrepancies may be observed (less than 0.5%).

The diagnosis was successful. Although only the catastrophic defects were diagnosed in this example, soft faults can be easily introduced. Accordingly, we may conclude that ANNs are convenient and powerful means for diagnosis, and, what is important, realisable as a hardware that may be as fast as necessary to follow the changes of the system's response in real time.

V. CONCLUSION

ANN approach is applied here, for the first time, to diagnosis of catastrophic defects in a digital part of nonlinear mixed-mode circuit. We consider this result as a full success. Although only the catastrophic defects were diagnosed in this example, soft faults can be easily introduced. Accordingly, we may conclude that ANNs are convenient and powerful means for diagnosis, and, what is important, realisable as a hardware that may be as fast as necessary to follow the changes of the system's response in real time.

Our future work will be devoted to implemetation of this idea to complete set of faults that include faults in analog and the digital part. Catastrophic as well as soft fauts are intended to be introduced.

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